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IN THE CLAIMS

Please amend claims 1 and 11 as follows:

1. (CURRENTLY AMENDED) A clock and data recovery circuit, comprising:

(a) a multi-phase voltage-controlled oscillator (VCO) for accepting a control signal and for changing a frequency of a 10 [[Gb/s]] GHz clock signal output from the [[VCO]] voltage-controlled oscillator in response thereto, wherein the voltage-controlled oscillator outputs a plurality of phases of the 10 [[Gb/s]] GHz clock signal;

(b) a phase detector (PD) for sampling a 40 Gb/s input data signal using the 10 [[Gb/s]] GHz clock signal received from the voltage-controlled oscillator and generating four 10 Gb/s output data signals in response thereto, wherein the 40 Gb/s input data signal is re-timed and de-multiplexed into the 10 Gb/s output data signals by the phase detector using half-quadrature phase offsets of the 10 [[Gb/s]] GHz clock signal, such that each of the 10 Gb/s output data signals detects an edge or transition in the 40 Gb/s input data signal and whether the edge or transition is early or late with respect to its corresponding half-quadrature phase offset of the 10 [[Gb/s]] GHz clock signal;

(c) a voltage-to-current (V/I) converter for converting the 10 Gb/s output data signals from the phase detector to a control current; and

(d) a loop filter (LPF) for integrating the control current from the Voltage-to-Current Converter and for outputting the control signal to the voltage-controlled oscillator in response thereto;

(e) wherein the multi-phase voltage-controlled oscillator, phase detector, voltage-to-current converter and loop filter are implemented in complementary metal-oxide semiconductor (CMOS).

2. (ORIGINAL) The clock and data recovery circuit of claim 1, wherein the circuit accepts a single input data signal, and re-times and de-multiplexes the input data signal to a plurality of output data signals.

3. (ORIGINAL) The clock and data recovery circuit of claim 1, wherein the phase detector uses half-quadrature phases of the clock signal provided by the voltage-controlled oscillator to sample the input data signal, thereby detecting the edges or transitions in the input data signal, and determining whether the clock signal is early or late.



PAGE 5/10 * RCVD AT 4/23/2007 2:48:35 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-5/9 * DNIS:2738300 * CSID:+13106418798 * DURATION (mm-ss):01-56

4. (ORIGINAL) The clock and data recovery circuit of claim 1, wherein the phase detector employs a plurality of flip-flops to strobe the input data signal at intervals based on the plurality of phases of the clock signal received from the voltage-controlled oscillator.

5. (ORIGINAL) The clock and data recovery circuit of claim 1, wherein the phase detector compares every two adjacent or consecutive samples stored by two adjacent or consecutive flip-flops by means of an associated XOR gate, which generates a net output current if the two adjacent or consecutive samples are unequal, thereby indicating that an edge or transition has occurred in the input data signal.

6. (ORIGINAL) The clock and data recovery circuit of claim 1, wherein the phase detector uses both leading and trailing edges of the phases of the clock signal to sample the input data signal, in order to detect the edges or transitions in the input data signal.

7. (PREVIOUSLY PRESENTED) The clock and data recovery circuit of claim 1, wherein the voltage-controlled oscillator is based on differential stimulus of a closed-loop transmission line at equally-spaced points that sustains a phase separation of 180° at diagonally-opposite nodes, providing 45° phase steps in between for the clock signal.

8. (PREVIOUSLY PRESENTED) The clock and data recovery circuit of claim 7, wherein the voltage-controlled oscillator's oscillation frequency is uniquely given by a travel time of a wave around the loop.

9. (PREVIOUSLY PRESENTED) The clock and data recovery circuit of claim 7, wherein inductor elements of the voltage-controlled oscillator are grouped into differential structures and -$G_m$ cells are placed in close proximity to the nodes of the voltage-controlled oscillator.

10. (PREVIOUSLY PRESENTED) The clock and data recovery circuit of claim 7, wherein each differential port of the voltage-controlled oscillator is buffered by an inductively-loaded differential pair of switches.



PAGE 6/10 * RCVD AT 4/23/2007 2:48:35 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-5/9 * DNIS:2738300 * CSID:+13106418798 * DURATION (mm-ss):01-56

11. (CURRENTLY AMENDED) A method of clock and data recovery, comprising:

(a) accepting a control signal into a multi-phase voltage-controlled oscillator (VCO) and changing a frequency of a 10 [[Gb/s]] GHz clock signal output from the voltage-controlled oscillator in response thereto, wherein the voltage-controlled oscillator outputs a plurality of phases of the 10 [[Gb/s]] GHz clock signal;

(b) sampling a 40 Gb/s input data signal at a phase detector (PD) using the 10 [[Gb/s]] GHz clock signal received from the voltage-controlled oscillator and generating four 10 Gb/s output data signals in response thereto, wherein the 40 Gb/s input data signal is re-timed and de-multiplexed into the 10 Gb/s output data signals by the phase detector using half-quadrature phase offsets of the 10 [[Gb/s]] GHz clock signal, such that each of the 10 Gb/s output data signals detects an edge or transition in the 40 Gb/s input data signal and whether the edge or transition is early or late with respect to its corresponding half-quadrature phase offset of the 10 [[Gb/s]] GHz clock signal;

(c) converting the 10 Gb/s output data signals from the phase detector to a control current at a voltage-to-current (V/I) converter; and

(d) integrating the control current from the Voltage-to-Current Converter at a loop filter (LPF) and outputting the control signal to the voltage-controlled oscillator in response thereto;

(e) wherein the multi-phase voltage-controlled oscillator, phase detector, voltage-to-current converter and loop filter are implemented in complementary metal-oxide semiconductor (CMOS).

12. (ORIGINAL) The method of clock and data recovery of claim 11, further comprising accepting a single input data signal, and re-timing and de-multiplexing the input data signal to a plurality of output data signals.

13. (ORIGINAL) The method of clock and data recovery of claim 11, wherein the phase detector uses half-quadrature phases of the clock signal provided by the voltage-controlled oscillator to sample the input data signal, thereby detecting the edges or transitions in the input data signal, and determining whether the clock signal is early or late.

14. (ORIGINAL) The method of clock and data recovery of claim 11, wherein the phase detector employs a plurality of flip-flops to strobe the input data signal at intervals based on the plurality of phases of the clock signal received from the voltage-controlled oscillator.



PAGE 7/10 * RCVD AT 4/23/2007 2:48:35 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-5/9 * DNIS:2738300 * CSID:+13106418798 * DURATION (mm-ss):01-56

15. (ORIGINAL) The method of clock and data recovery of claim 11, wherein the phase detector compares every two adjacent or consecutive samples stored by two adjacent or consecutive flip-flops by means of an associated XOR gate, which generates a net output current if the two adjacent or consecutive samples are unequal, thereby indicating that an edge or transition has occurred in the input data signal.

16. (ORIGINAL) The method of clock and data recovery of claim 11, wherein the phase detector uses both leading and trailing edges of the phases of the clock signal to sample the input data signal, in order to detect the edges or transitions in the input data signal.

17. (PREVIOUSLY PRESENTED) The method of clock and data recovery of claim 11, wherein the voltage-controlled oscillator is based on differential stimulus of a closed-loop transmission line at equally-spaced points that sustains a phase separation of 180° at diagonally-opposite nodes, providing 45° phase steps in between for the clock signal.

18. (PREVIOUSLY PRESENTED) The method of clock and data recovery of claim 17, wherein the voltage-controlled oscillator's oscillation frequency is uniquely given by a travel time of a wave around the loop.

19. (PREVIOUSLY PRESENTED) The method of clock and data recovery of claim 17, wherein inductor elements of the voltage-controlled oscillator are grouped into differential structures and $-G_m$ cells are placed in close proximity to the nodes of the voltage-controlled oscillator.

20. (PREVIOUSLY PRESENTED) The method of clock and data recovery of claim 17, wherein each differential port of the voltage-controlled oscillator is buffered by an inductively-loaded differential pair of switches.



PAGE 8/10 * RCVD AT 4/23/2007 2:48:35 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-5/9 * DNIS:2738300 * CSID:+13106418798 * DURATION (mm-ss):01-56